**REPORT ON 4-BIT ARBITER PUF IN ALTERA**

**INTRODUCTION:**

Designing a 4-bit arbiter puf in altera DE2- 115 cyclone 4 Board.

**DESIGN:**

**A picture containing different

Description generated with high confidence**

Fig 1: Schematic of 4-bit arbiter PUF

This is the design of 4 bit arbiter puf. The internal structure of mux one symbol is shown in Fig2. We have multiplexers placed in top as well as bottom while they share the same inputs and the select lines. The select lines are used as Challenge for the PUF.

A picture containing screenshot

Description generated with high confidence

Fig 2: Schematic of mux\_one\_symbol

When the model is transferred to the FPGA Board, we get different results in the arbiter PUF when checking in different logic regions.

**RESULTS:**

**1st test:**

Pin Planner:

S1= Pin\_Y23 S2=PinY\_24 S3=Pin\_aa22 S4=Pin\_aa24

Challenge: -

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S1** | **S2** | **S3** | **S4** | **Output(G-19)** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**2nd Test**

S1 = Pin\_AB28 S2= Pin\_AC28 S3= Pin\_AC27 S4= Pin ­\_AD27

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S4** | **S3** | **S2** | **S1** | **O/P** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Both are embodied in different logic cells due to the nature of the circuit, we get different result for the same circuit.**